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Low Power CMOS Design Technique for Power Switches Gating.

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ABSTRACT

Power-gating is a low-power design technique to reduce leakage power. It has gained popularity in sub-100-nm CMOS designs, where leakage power is a major contributor to the overall power consumption. It utilizes power switches to power-down the logic blocks during the idle mode to reduce leakage power consumption. Power switches are used as a part of the power-gating technique to reduce the leakage power of a design. To the best of our knowledge, this is the first report in open literature to show a systematic diagnosis method for accurately diagnosing power switches. The proposed diagnosis method utilizes the recently proposed design-for-test solution for efficient testing of power switches in the presence of process, voltage, and temperature variation. It divides power switches into segments such that any faulty power switch is detectable, thereby achieving high diagnosis accuracy. This paper proposes that the analysis of Fine grain technique and Coarse grain techniques and result will be done by using the Tanner EDA tool 13.0, and calculate the power consumption.

Keywords: CMOS, Power-Gating, VLSI, Fine grain, course grain

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INTRODUCTION

Distributed generation is an acceptance of gaining for domestic customer who has huge number of small-scale generation units such as wind turbines, photovoltaic cells or fuel cells. With the purpose of connect these respective power electronic systems to the grid, prominent gating synchronization of all power switches must be performed. Thus, the time delays and zero crossing detectors has been utilized to achieve this task for many years as the method of primary synchronization on both three and single phase systems, but the delay has depends only on frequency. To overcome this issue, Arctangent gating method can be used [1-4], but this method is especially developed for three-phase systems. The techniques for single phase zero crossing measurement that combines both software and hardware techniques with low process delay [5]. In spite of this, the phase errors required post-processing and pre-processing so that it is decreased to acceptable levels. Synchronizing Thyristor based gating power converters has been used for fits system and online adaptive waveform reconstruction, where the frequency of the line may vary [6]. Synchronous PLLs has been utilized for control the AC system which is applicable for standard execution in three-phase applications [7-9].

Attenuators has been extensively used in modern communication systems for control gain [10-13]. In relation with the variable gain amplifiers (VGAs) are conventionally utilized as a gain control in circuits, the attenuators reveal food performance in power efficiency, linearity, phase variation and control complexity [14-16]. The traditional attenuators can be classified into distributed and switched topologies. The distributed attenuators have less compact structure and give low attenuation range rather than switched attenuators.

In digital VLSI circuits, power consumption is an important factor. More power consumption may affects circuit reliability and shorten circuit lifetime or runtime errors [17]. Numerous power estimation techniques have been implemented; they can particularly be classified into two important categories. First methods are belongs to non-simulation based techniques which mainly related to probabilistic measures for the switching and the inputs activities for find the consumption of power [18-24]. Second, simulation-based techniques which depend on simulating the circuit with a prominent set of inputs for obtain the consumption of power [25-29].

In the present work, the proposed diagnosis method utilizes the recently proposed design-for-test solution for efficient testing of power switches in the presence of process, voltage, and temperature variation. It divides power switches into segments such that any faulty power switch is detectable, thereby achieving high diagnosis accuracy. Finally the analysis of Fine grain technique and coarse grain techniques and result will be done by using the Tanner EDA tool 13.0, and calculate the power consumption.

PROPOSED SYSTEM

The DFT proposed in achieves fast test time through balanced charge and discharge times and eliminates the possibility of a false test.

Circuit Diagram

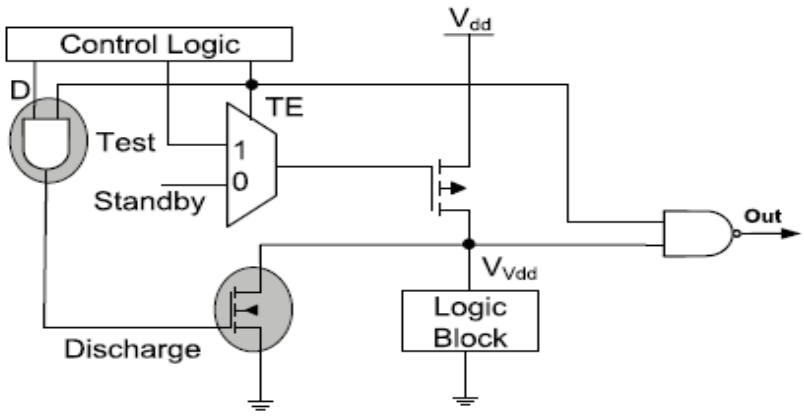

Fig 1: Fine grain Design

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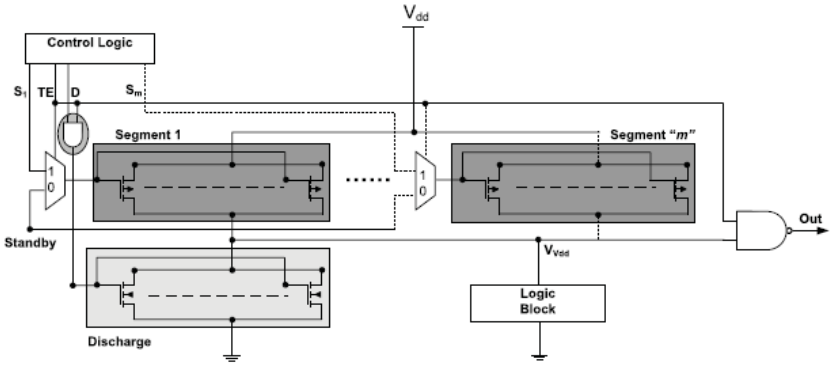

Fig 2: Coarse Grain Design

Power gating is a low-power design technique to reduce leakage power. It has gained popularity in sub-100-nm CMOS designs, where leakage power is a major contributor to the overall power consumption. It utilizes power switches to power-down the logic blocks during the idle mode to reduce leakage power consumption. Power switches are implemented as header switches or footer switches. This paper analyzes headers in detail, but the results are equally applicable to footer power switches as well. Power switches are usually implemented in either "fine-grain" or "coarse-grain" design styles as shown in Figure 1 and 2. A fine-grain style incorporates a power switch within each standard logic cell with a control signal to switch on/off the power supply of the cell. In the coarse-grain design style, a number of power switches are combined to feed a block of logic. When comparing the two design styles, the fine-grain design simplifies the incorporation.

Of power gating through existing EDA tools, but it has a higher area overhead and is more vulnerable to voltage drop fluctuations due to process, voltage, and temperature (PVT) variations. Therefore, the coarse-grain design style is a more popular design choice in practice and is the focus of this paper. Power switches are implemented in two power modes, which provides a tradeoff between leakage power saving and wake-up time. These include complete power-off mode (higher leakage power saving) and intermediate power-off mode (lower wake-up time). Design-for-test (DFT) solutions for power switches with intermediate power-off mode have been recently proposed . Therefore; this paper focuses on power switches with a complete power-off mode.

TANNER SOFTWARE DESCRIPTION

Today's semiconductors and electronic systems are complex that designing them would be impossible without electronic design automation (EDA). This primer provides a comprehensive overview of the electronic design process, and then describes how design teams use Cadence tools to create the best possible design in the least amount of the time.

Figure 3 provides specification of proposed design. This step involved stating in definite terms the performance of the chip. Like if we are making a processor, data size, processor speed, special functions, power etc. is clearly stated at this point. Also somewhat it is decided, the way to implement the design. So, it deals with architectural part of the design at highest level possible.

HDL: Hardware Description Language is used to run the simulations. It is very expensive to build the entire chip and then verify the performance of the architecture. Imagine if after designing a chip for a whole year, the chip fabricated, does not come even closer to the stated specifications. Hardware description languages provide a way to implement a design without going into much architecture, simulate and verify the design output and functionality.For eg. Rather than building a mux design in hardware, we can write Verilogcode and verify the output at higher level of abstraction.

Examples of HDL: VHDL, Verilog HDL

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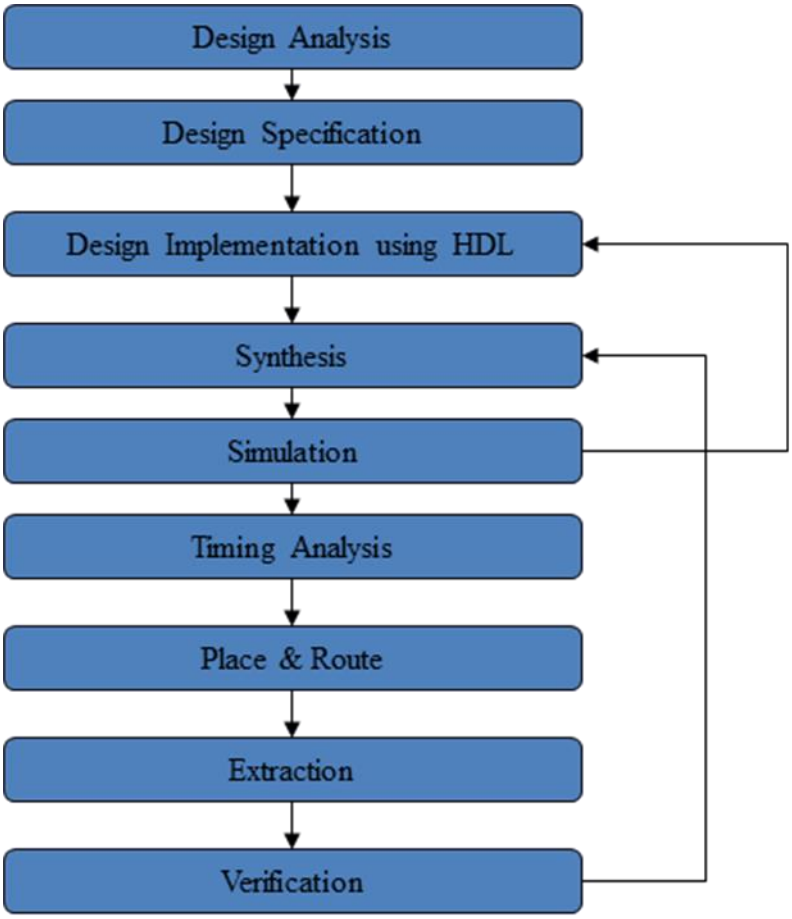

Fig 3: Design Specification:

Tanner EDA Design Tools:

- S-edit - a schematic capture tool
- T-SPICE - the SPICE simulation engine integrated with S-edit
- W-edit - waveform formatting

Tanner Tools:

- Tanner EDA is a suite of tools for the design of integrated circuits.
- Tanner EDA is mainly used to analyze circuits at switch level & gate level.
- These are tool used to ;
  - enter schematics
  - perform SPICE simulations
  - do physical design (i.e., chip layout)
  - Perform design rule checks (DRC) and layout versus schematic (LVS) checks.

S-EDIT:

- S-Edit is a powerful design capture & entry tool that can generate netlists directly usable in T-Spice simulations.
- Provides an integrated environment for editing circuits, setting up and running simulations and probing the results.
- It also provides the ability to perform SPICE simulations of the circuit
- These circuits that can be driven forward into a physical layout.

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T-SPICE:

- It is a complete design capture and simulation solution that provides accuracy.
- The role of T-Spice is to help design and verify a circuit's operation.
- T-Spice simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication.
- Performs fast, accurate simulations for analog and mixed-signal IC designs and fully supports foundry models for reliable and accurate simulations.

T-SPICE vs SPICE:

- T-Spice uses an extended version of the SPICE, compatible with all industry-standard SPICE simulation programs.
- Speed: T-Spice provides highly optimized code for evaluating device.
- It also provides the option of table-base transistor model evaluation which yields dramatic increase simulation speed.

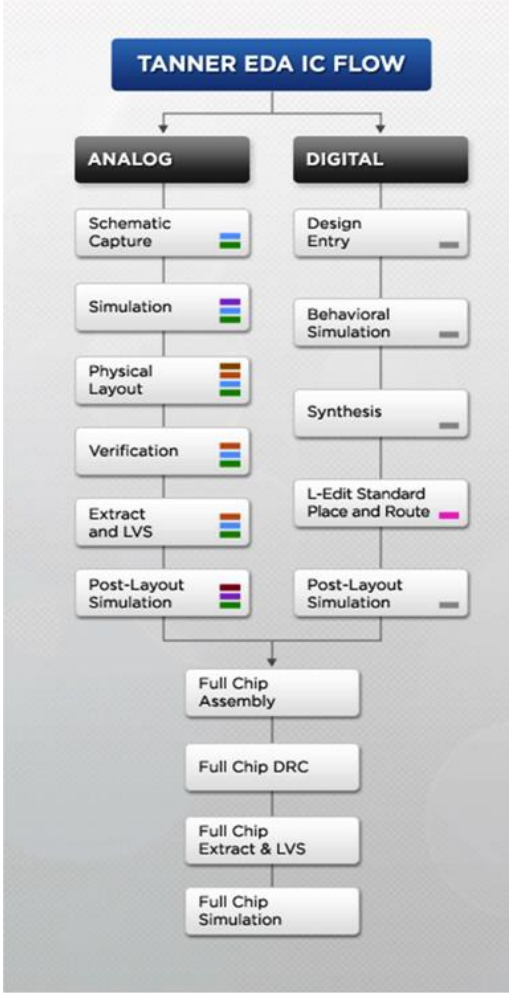

Fig 4: Tanner EDA IC flow

RESULTS AND DISCUSSION

Procedure for Measurement

The test chip in fabricated in a standard six metal 130-nm CMOS process occupying an area of 790-by-470 μm. The chip was packaged in a surface mount case and soldered on a printed circuit board, which provides all DC and RF connections. The VCO is buffered by on-chip open drain amplifiers, which are not

included in the total current consumption. Power supply on the PCB is bypassed with surface mounted tantalum and ceramic capacitors. All phase noise values are measured with HP4352S signal source analyser through a divide-by-2 circuit. Phase noise improvement of 6 dB due to frequency division is removed from the measurement results. Operating voltage *VDD* is set to 2.8 V with the regulator dropping it to between 2.3 and 2.45 V at *V*CORE depending on oscillation frequency. Measured current consumption across the entire coarse tuning range is between 7.3 and 10.6 mA, shows the output frequency across the entire coarse tuning range. The tuning range is from 3015 to 5298 MHz. The measured voltage at *V*CORE and the current consumption versus oscillation frequency are shown in Fig. 10. The measured phase noise results at 1- and 3-MHz offsets for the entire tuning range or better phase noise performance at all oscillation frequencies at 1-MHz offset. The performance is comparable to recently published VCOs with a similar tuning range.

IC Design

Physics students with a sound theoretical knowledge of solid state physics and semiconductor technology are not usually introduced to IC *design* and are completely unable to design the simplest device. This is not a reflection of the importance but rather the lack of IC design experience outside electrical engineering departments. Semiconductor technology continues to attract enormous investment and is available to anyone with the know-how to use it. It is used not only to design complex high density circuits but also chemical and medical sensors, ASICS (application specific integrated circuits) of many types e.g. focal plane detectors.

IC design requires an understanding of the fabrication process, digital electronics and makes use of a range of important CAD tools as listed below. The objective of this course is to illustrate the complete design cycle and produce a fully verified simple design ready for fabrication. This will provide literacy in one of the dominant technologies of the time. This introduction will not make you into a designer but will give you literacy in the area of integrated circuit design which is lacking in most physicists.

SPICE Simulation Setup in S-Edit

Prior to running the T-Spice simulation, the analysis commands and all processing options need to be established. This is accomplished using the Setup SPICE Simulation dialog in DxDesigner.

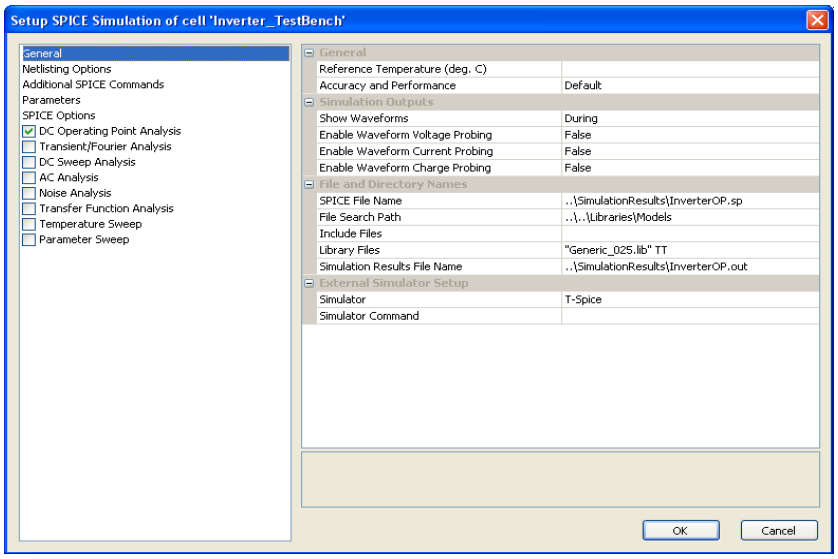

Fig 5: Setup for Simulation of Cell "inverter_TestBench"

Export the Netlist to T-Spice

- In the inverter_Testbench Operating Point schematic, use Tools > Design Checks to execute the Design Checker.

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- The Design Checker will display any violation or errors in the Command window. There should not be any errors in the file inverter_Testbench Operating Point.
- Press the T-Spice icon ( ) to export a T-Spice netlist file named inverterOP.sp.
- DxDesigner will launch T-Spice with the inverterOP.sp netlist open.

DC Operating Point Analysis

DC operating point analysis finds a circuit's steady-state condition, obtained (in principle) after the input voltages have been applied for an infinite amount of time. Two transistors, MP1 and MN1, are defined in inverterOP.sp. These are MOSFETs, as indicated by the key letter M that begins their names. Following each transistor name are the names of its terminals in the required order: drain–gate–source–bulk. Then the model name (PMOS or NMOS in this example) and physical characteristics, such as length and width, are specified.A capacitor CC1 (signified by the key letter C) connects nodes N 1 and GND with a capacitance of 1p.Two DC voltage sources are defined: VVin, which sets node N2 to 1.0 volt relative to ground and VVpower, which sets node Vdd to 3.3 volts as defined by the variable Vpwr.

- Notice that the simulation settings which were entered in the SPICE Simulation Setup dialog resulted in .option, .lib, and .op commands being written to the T-Spice input file. The .lib command causes T-Spice to read the contents of the Generic_025.lib library file for the evaluation of transistors MP1 and MN1, and the search option identifies the path to the library files. In this case, the library file contains two device .model commands, describing MOSFET models PMOS and NMOS, as shown below for PMOS:

Transient Analysis—Inverter

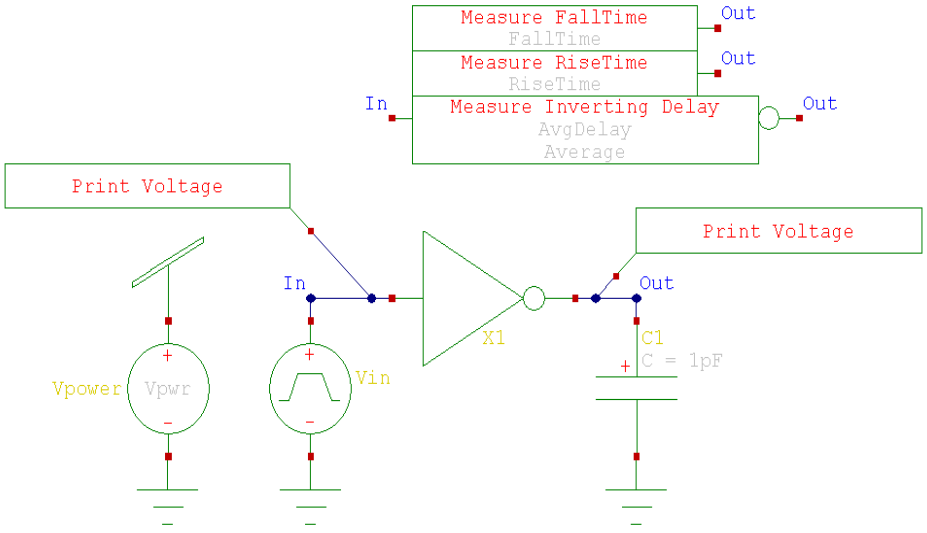

Fig 6: Schematic diagram for T-Spice Input

Transient analysis provides information on how circuit elements vary with time. The basic T-Spice command for transient analysis has three modes. In the *op* mode (default), the DC operating point is computed, and T-Spice uses this as the starting point for the transient simulation. Schematic diagram for T-Spice input as shown in Figure 6.

This circuit is similar to that of Inverter, except that voltage source VVin here generates a pulse, rather than setting a constant value. The times and voltages that define the "legs" of the waveform are specified in the arguments to pulse. The initial current is zero amperes and the peak current is Vpwr, with an initial delay of zero seconds. The rise and fall times are one nanosecond, with a pulse width of 49 nanoseconds and a pulse period of 100 nanoseconds. The ".tran"command specifies the characteristics of the transient analysis to be

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performed. The maximum time step allowed is 250 Pico with a total duration of 300 nanoseconds as shown in Figure 7.

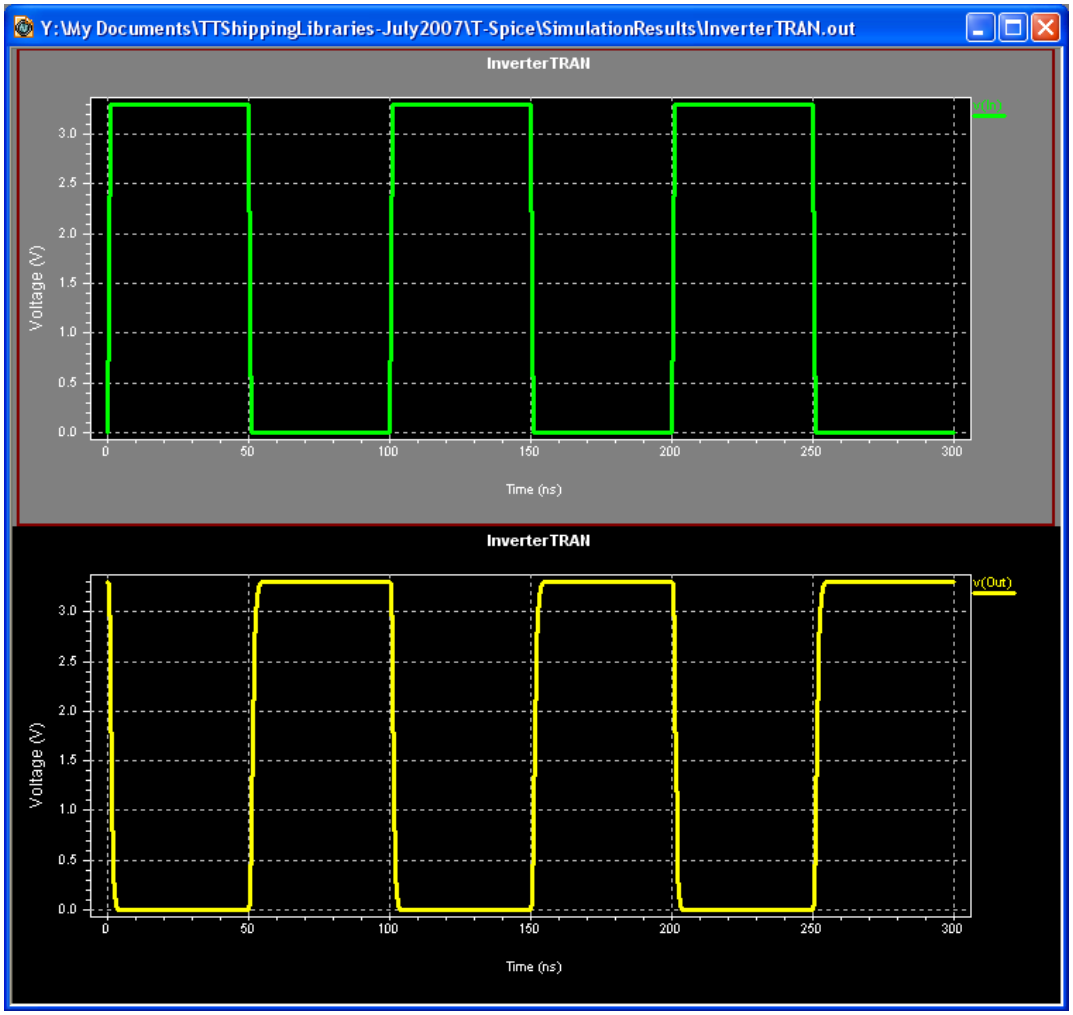

Fig 7: Voltage Vs Time of Inverter TRAN.

CONCLUSION

In conclusion, the proposed diagnosing switches has gained popularity in sub-100-nm CMOS designs, where leakage power is a major contributor to the overall power consumption. It is utilized power switches to power-down the logic blocks during the idle mode to reduce leakage power consumption. Power switches are used as a part of the power-gating technique to reduce the leakage power of a design. The systematic diagnosis method for accurately diagnosed with power switches. The proposed diagnosis method utilized in design-for-test solution for efficient testing of power switches in the presence of process, voltage, and temperature variation. Power switches are divided into segments such that any faulty power switch is detectable, thereby achieving high diagnosis accuracy. This paper proposed that the analysis of Fine grain technique and coarse grain techniques and result have been done with the help of Tanner EDA tool 13.0, and calculated the power consumption.

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